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Mux/Demux Testing with Agilent 81250 ParBERT

Mux Demux parts are important for the communication. These parts care for transmitting and receiving data over transmission links, which could be electrical or optical.On the other side the data is available on a bunch of parallel lines at much lower speed for further processing.

This presentation deals with testing electric devices in R&D and Manufacturing.

Issues

- Application
- Serializer / De-Serializer Architecture
- Obstacles of today's testing
- The better way:
  PRBS and PRWS data, Synchronization
- Measurements in R&D and Manufacturing
- 3 Examples

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This presentation deals with these issues.

1. We look to the application areas

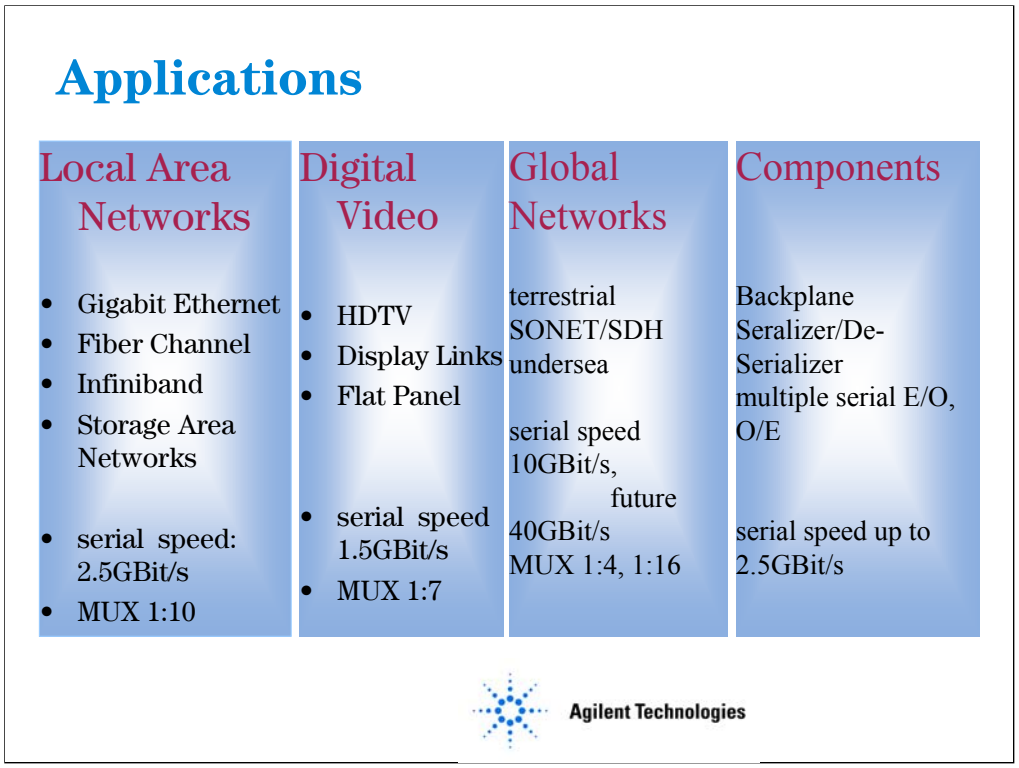
2. We look at the generic architecture and discuss an example to understand function and points of interest from the view of testing such parts

3. We deal with the obstacles of traditional TEST APPROACH

4. We discuss the important elements to overcome these obstacles

5. We look more closely on the test requirements with the eyes of the designer and the production test engineer

6. We look in detail on the scenarios of three different implementations



The areas for using such parts are:

- Local Area Networks
- Digital Video
- Global Networks

Within the Local Area Networks, the applications are

Gigabit Ethernet

Fiber Channel

Storage Area Networks

These applications work with a serial speed of 2.5Gbit/s and typically the MUX ratio is 1:10

The Digital Video applications are

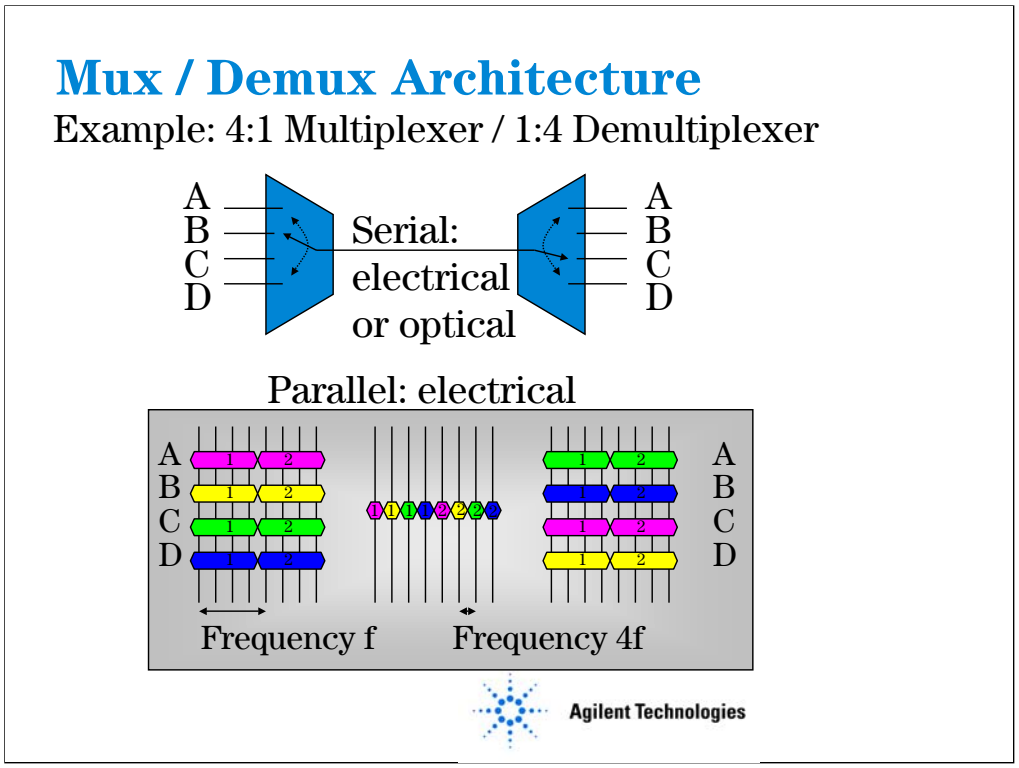
HDTV

Display Links

Flat Panel Interface

Here the serial speed is today up to 1.5Gbit/s with a typical MUX ratio of 1:7. The total bandwidth of such a link is often much higher, but this results of having several serial lines combined.

The global networks are terrestrial or undersea with SONET / SDH protocol. Here the serial speeds are 10Gbit/s with possible 40 GBit/s in future. The MUX ratio is 1:4 and 1:16.



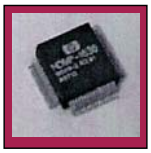
Mux Demux parts care for collecting and distributing data which are transmitted over electrical or optical links.

On the transmitter side (TX) the information is collected from a bunch of parallel lines and put one line with speed up of 1:4, 1:7, 1:10 1:20 against the parallel side with help of the MUX circuitry.

On the receiver side (RX) the DEMUX circuitry will receive the high speed data and convert to a parallel bus so that following protocol Asics can process it at slower speed.

Figure 1 shows an example for a 1:4 implementation, so the frequency on the serial side is 4 times faster. This simple picture does not care on latency issues, but be aware already that on the receiver side the parallel data may be cyclically shifted.

Fiber Channel / Gigabit Ethernet



HDMP-263x from:

Agilent Technologies
Innovating the HP Way

Functional Description :
single bipolar circuit with TX and RX
QFP package, 64 pin
low cost physical layer solution, up to 2.5 Gbit/s
10 bit wide for 8B/10B coding
Receiver synchronizes on ‘comma’ character

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Gigabit Ethernet/ Fiber Channel Implementation (1)

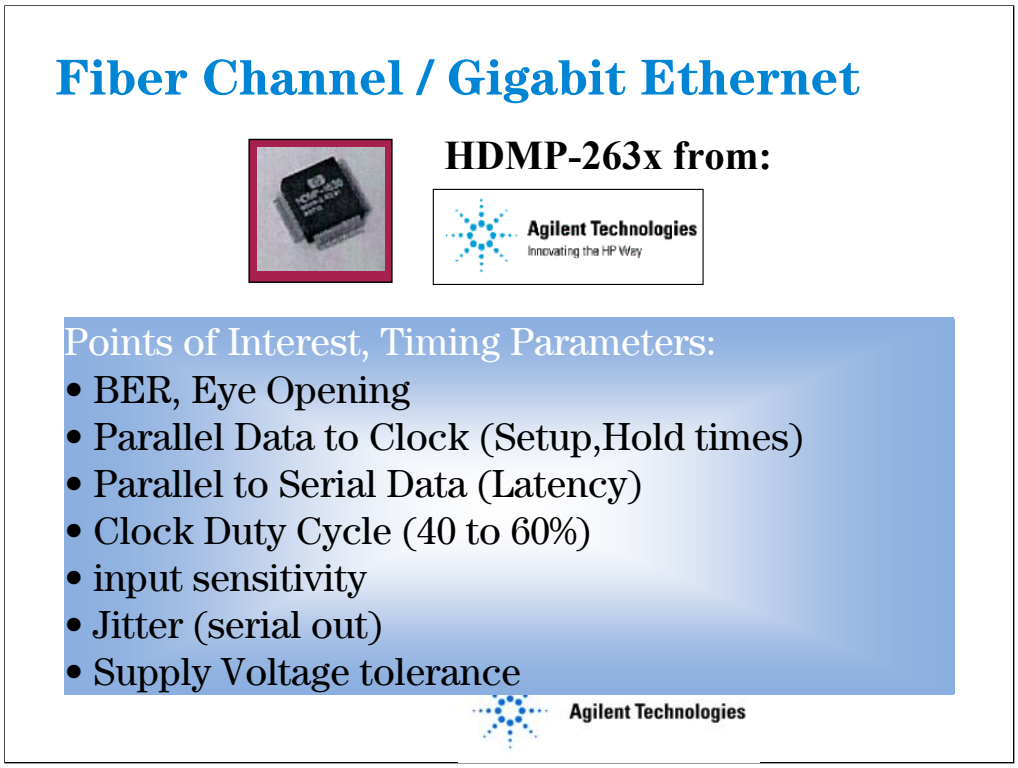
There are silicon bipolar integrated transceivers from several vendors on the market. This presentation reflects on Agilent’s HDMP-263x chip.

This comes in a 64 pin QFP package as a low cost physical layer solution.

•Serializer and De-serializer are in one package.

•The parallel side is 10 bit wide for 8B/10B coding.

• The receiver synchronizes the parallel outputs on ‘comma’ character.



Gigabit Ethernet/ Fiber Channel Implementation

When looking to the data sheet, these are the points of interest:

•BER, Eye opening

•Parallel Data to Clock (setup- / hold time)

▪Parallel to Serial Data (latency)

▪Clock Duty Cycle

▪Supply Voltage tolerance

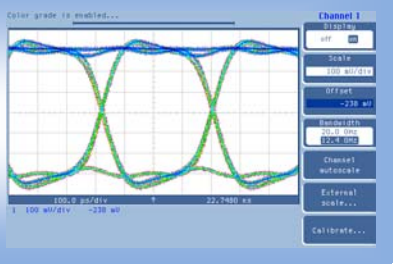
▪Input sensitivity, Output signal (Eye diagram)

▪Jitter (serial out)

Within the Appendix there are two more MUX/DEMUX examples from other Application Areas. The points of interest are mostly similar except these examples work at different speeds.

R&D vs. Manufacturing

Points of Interest,
Example: Eye Opening



- need to test the same, but:

R&D:
- Characterization
  - Iso BER
  - transition times
  - jitter

Manufacturing:
- meet the spec
- fast, throughput

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Basically R&D and Manufacturing have to care for the same points of interest, so the have to test for the same timing parameters. But the intention is totally different:

R&D has first to verify if the design works as anticipated, so the question is:

Does the device work as desired? This question is often answered without testing as this is a matter of simulation.

Secondly the question is where are the limits and what are the margins. So the question is:

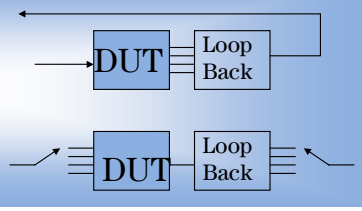
How well does the device work.

These kind of testing is called ‘Characterization’ and it is a time consuming task as a lot of measurements have to be performed as dependency of other parameters. Environmental issues like operating voltage and temperature belong also to this chapter.

Manufacturing has to verify the specs on each individual part. And throughput is essential. So they have to measure same parameters but methodology will be totally different. So the question is to check if the individual part meets the spec. And this should be done as fast as possible

How the test is done today

- Loop Back
- one channel at time



- Need golden device, what if it gets marginal?
- Need of add. silicon for testability
- Channel by channel is time consuming & not real world stress

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The traditional test approach is built on loop back or/and test one channel at the time. This is achieved with help of 'Golden Devices' and/or there is additional silicon for testability.

1. Loop back is a method of converting the data from a certain port by the means of auxiliary circuitry to another port. So the parallel port will be mapped to a serial port again and so the testing can be achieved from and to normal mode, but the there is additional design work and redundancy in the chip just for test.

A Golden Device is the part which inverts the DUT functionality , so testing between similar interfaces can be achieved. Maintaining a Golden device is a costly issue, especially to trace that it does not gets marginal is not an easy task. Other approach is to embed the loop-back function into the silicon, so one can special testability operating modes.

2. Testing Channel by channel in a parallel architecture is possible and delivers good results. In R&D it is for sure a valid approach for functional verification. But it has it's limits regarding 'real world stress', which includes cross-talk or ground bounce due to simultaneously switching outputs. In manufacturing it is contra-productive regards of throughput.

The better way

81250 ParBERT:
"The Only Parallel Bit-Error-Rate Solution up to 0.66/1.3/2.6 GBit"

- Parallel & Modular
- PRBS, PRWS
- Synchronization
- Individual Timing / Levels per Channel
- differential inputs and outputs (LVDS)

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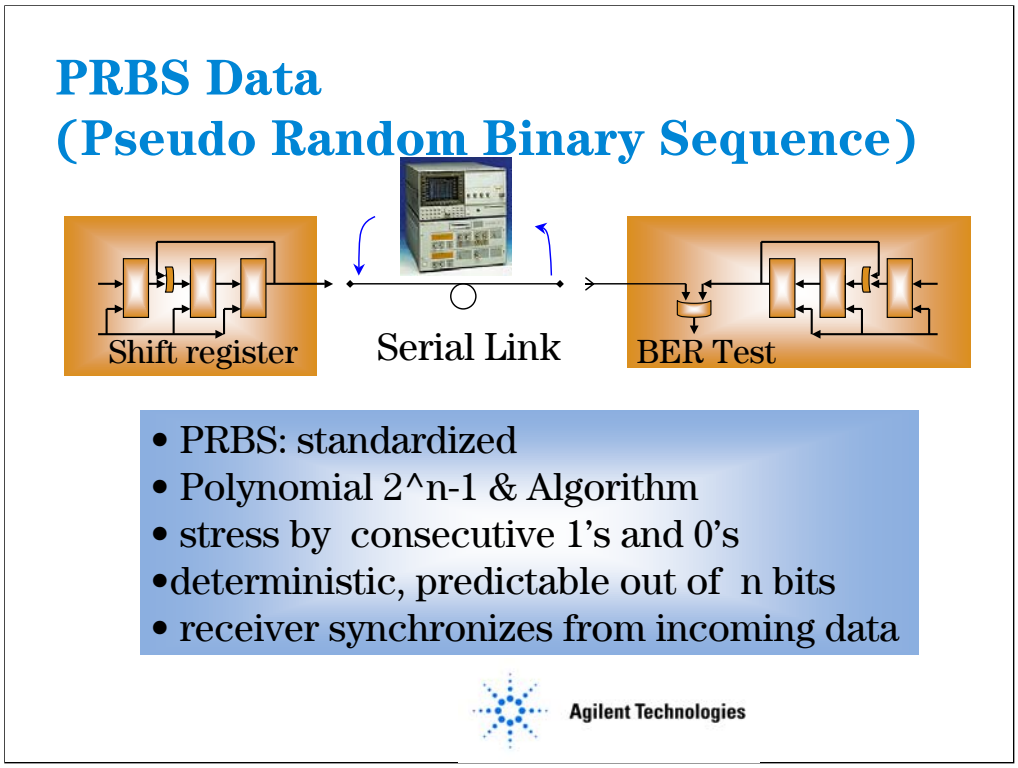
The better way for MUX Demux testing

1. Parallel BER test,
2. PRBS/PRWS together with synchronization
3. Individual timing and levels to make timing changes for and back possible to check for setup / hold times and propagation delay
4. Differential signals e.g. LVDS technology



What is PRBS:

For testing the physical layer the industry has established the 'Pseudo Random Binary Sequence' (PRBS). This is standardized by ANSI / ITU / CCITT.

It is defined by the polynomial 2^n-1 and a recurring algorithm. A shift register with internal feed-backs defining the algorithm is used for generation of the stimulus data stream.

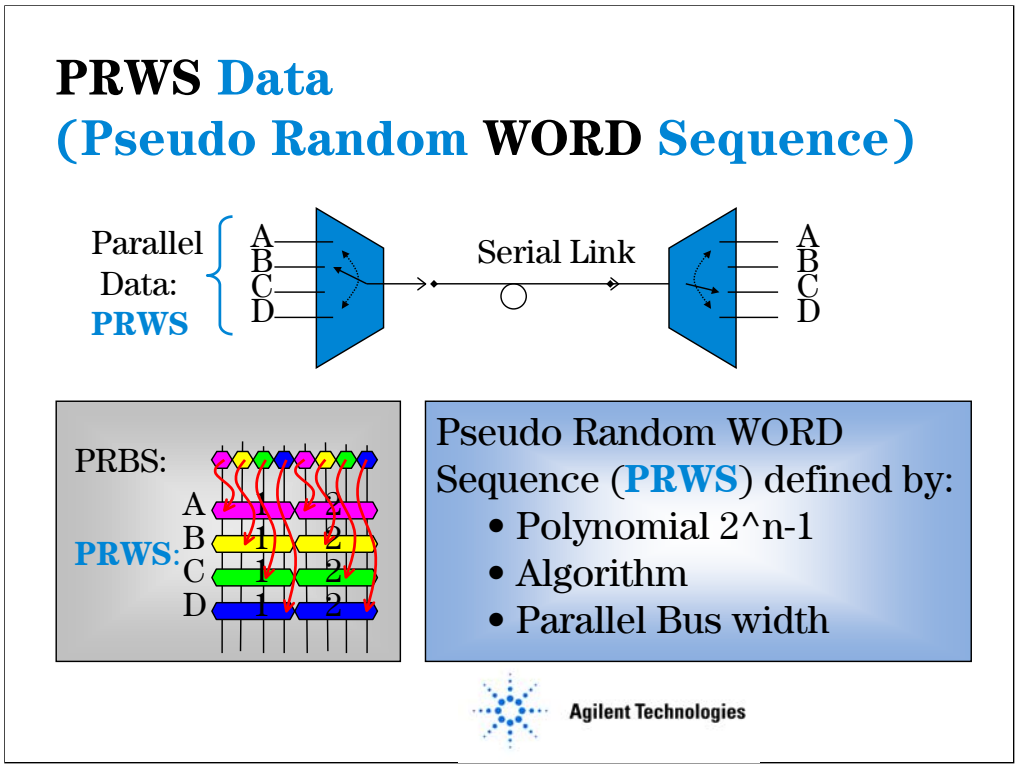
On the analyzer side the same register with same feedback's is used. For a certain time this will listen to the incoming data stream and then start to generate the further data to be used as expected data to check the incoming bits.

The data stream is deterministic as by capturing n bit failure free, one can predict the future signal. So a receiver can be synchronized for BER measurement out of running data stream. There is no need to know of start or synchronization signal from the stimulating side.

PRBS provides well-defined stress to the device under test (DUT) by defined maximum number of consecutive 1's and 0's.

The Gigabit Ethernet community recommends the use of 2^7-1. The SONET/SDH business has standardized on the use of PRBS 2^23-1.

As higher the polynomial gets, as more consecutive '0's and '1's appear, which is stress for the clock recovery circuits. Often it is desired to extend the max. number of same bits or to insert one or more errors to the bit stream. In this case memory is needed as the shift register cannot do this job.



What is PRWS:

Pseudo Random word sequence (PRWS) is an extension to PRBS. It is defined by

- Polynomial 2^n-1
- Algorithm
- Parallel bus width

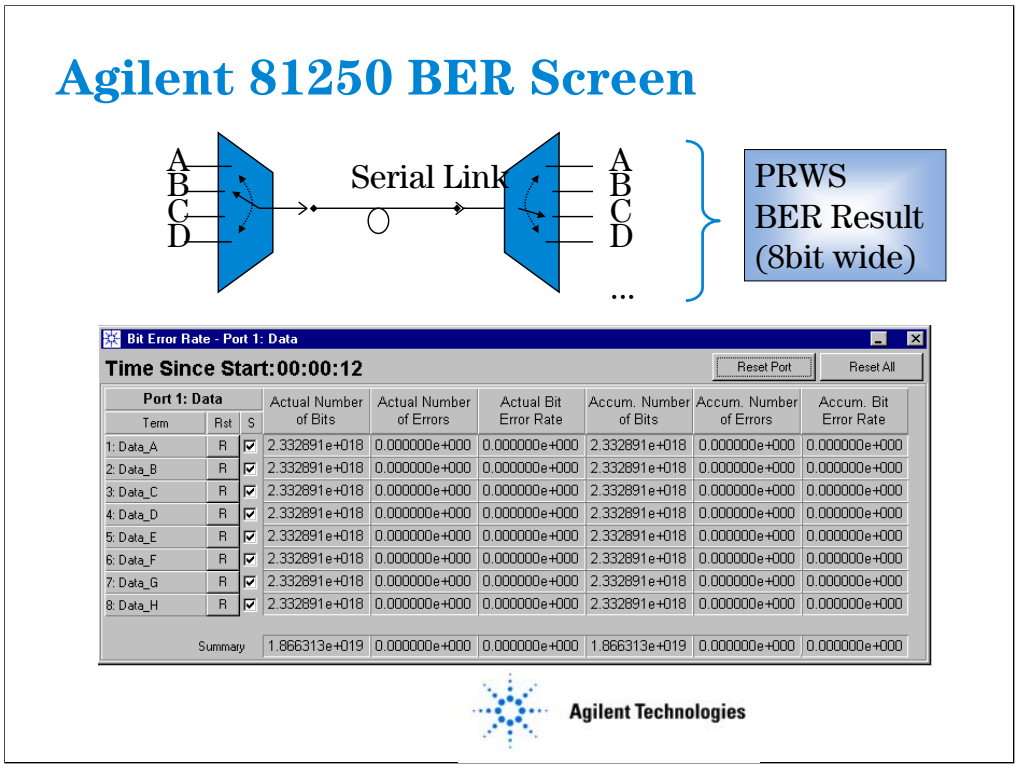
The bits of the PRBS will be assigned to the parallel lines the way that after multiplexing together it is an PRBS. Vice versa PRBS applied to an DEMUX will deliver PRWS.

There are in principle no limits for the port size on the parallel side. The PRWS can be generated from similar shift registers as the PRBS. There are only a few exceptions of port sizes and algorithms which are not possible. For the most polynomials in practical use (2^7-1, 2^23-1), there are few limitations only.

The benefit:

A test system which handles PRBS and PRWS allows BER Testing:

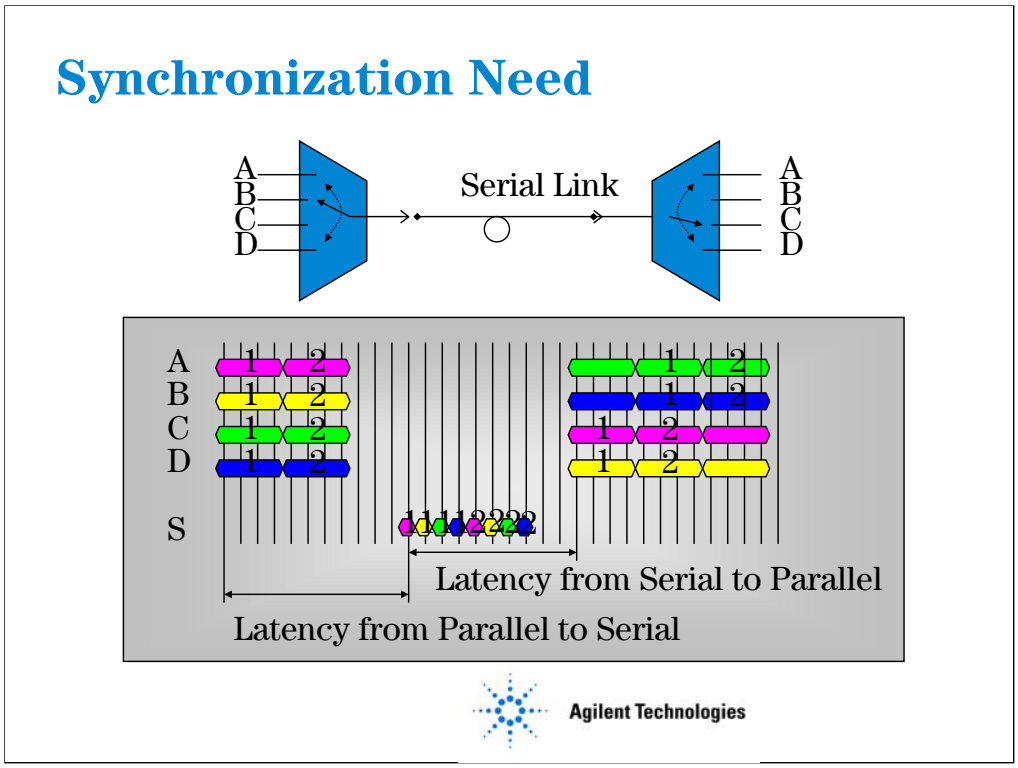
- Parallel to Serial
- Serial to Parallel
- Parallel to Parallel
- Multiple Serial to Multiple Serial



This is the result of BER test on a 8 bit wide parallel port of a DEMUX chip.

The 8 bit wide port is displayed with actual and accumulated results of number of vectors processed, number of errors occurred and calculated BER out of that. Finally there is a summary done over all lines.

Actual means the result which is periodically updated, Accumulated means since measurement is started.



Now we start to discuss about synchronization.

To do any BER measurement, it is necessary to compare the incoming data stream to expected data. The BER is then the ratio of bad bits versus all received bits.

PRBS/PRWS has the advantage that as soon as there is a short piece of stream available, one can predict how this stream continues. This assumes that you know the algorithm. So this short stream will be loaded into the register and after that you just clock it and so it will output the further stream. This can be used than as the expected data.

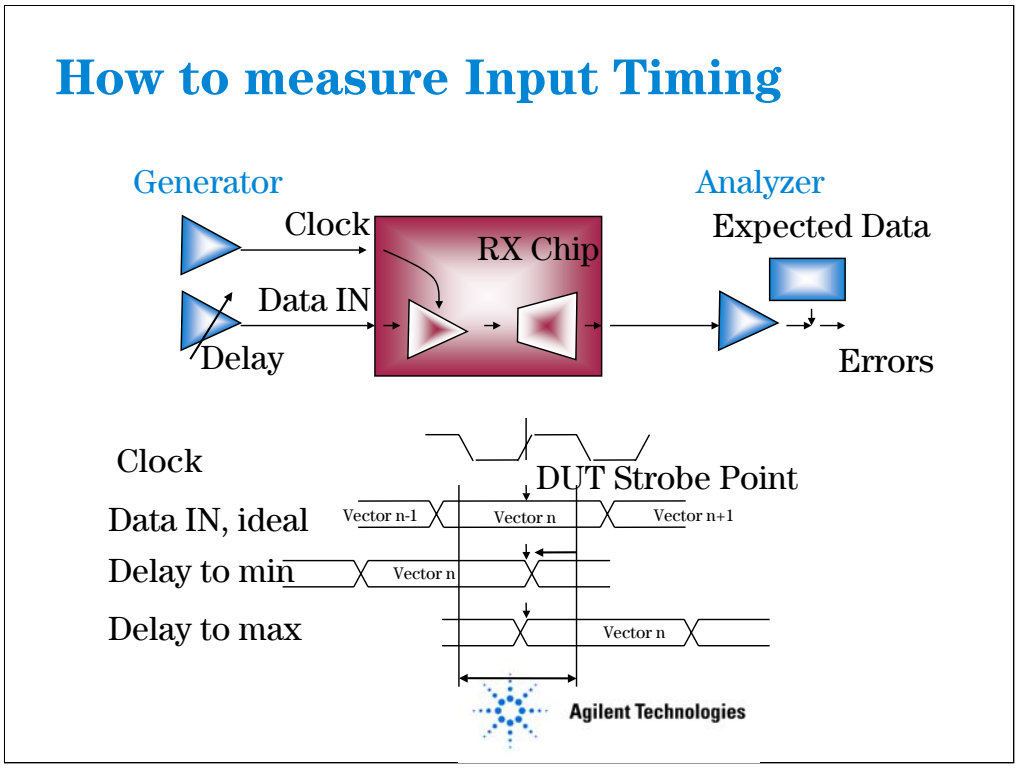
This operation is called ‘bit synchronization. So the test system will load the register, and then start checking the BER. If it is below a given figure, the synchronization was successful..

This works properly even it is not known when a DUT will send it’s output. So the synchronization works virtually unlimited time range.

But the relation between input and output timing is lost, it is just an unknown number of cycles in between.

Another principle of synchronization will be the ‘auto delay adjust’:

this makes use of a timing system which can change the sampling point at runtime. So the absolute timing relation is maintained after matching incoming and expected data . Such a timing system offers this capability within a limited range only.



To make measurements on Input or Output Timing, the DUT has to be stimulated with clock and data and the DUT output has to be compared against expected data. This data can be PRBS/PRWS or any other memory based bits.

With a nominal or ideal timing the DUT will strobe the input data. As a result the output data will match with the expected ones. The analyzer does this comparison from cycle to cycle. In this case the Analyzer will not see any error.

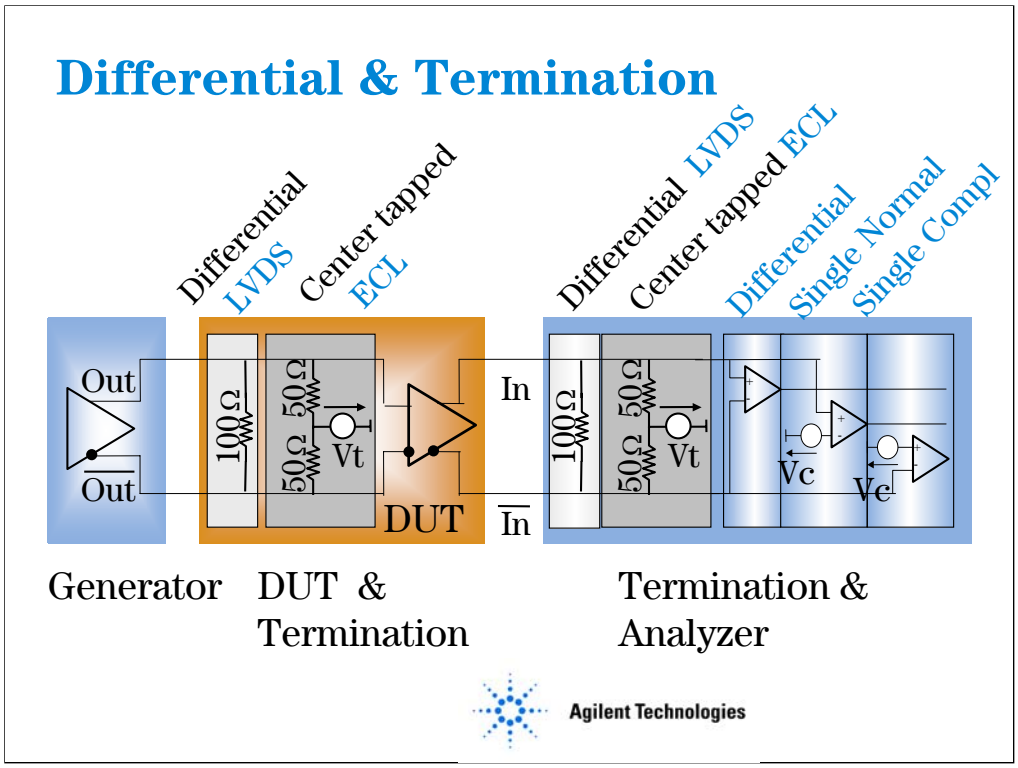
Now the input timing is measured by moving the timing of the input data around in reference to the input clock.

Still the analyzer will strobe the outputs at nominal timing and performs error counting.

As soon as the input data timing gets marginal, the device will strobe unreliable or even wrong as it strobes data belonging to the earlier/later cycle. Result is bunch of errors as expected and output data do no longer match.

So there is a certain window from minimum to maximum delay in reference to the clock timing where no errors occur. Delay to minimum defines the HOLD time, delay to maximum defines the SETUP time.

For output timing measurements the analyzer delay will be used to check the window of error free operation.



Differential technology is very widely used together with MUX/DEMUX circuitry. Differential means that there is an Output/Input together with complementary Input/Output. The complementary one always deals with the logical opposite of the normal one. So there will never happen same logical level on both, they always will be opposite or complementary (as long as nothing is broken).

LVDS (Low Voltage Differential Signaling) is a relatively new technology. This works with the 'Differential Termination' which is just a 100 Ohm resistor across the two signal lines. Be aware that termination is always done at the end of the lines to avoid reflections.

ECL/PECL is a common technology used for decades. This applies center tapped termination where a termination voltage source (Vt) is connected to the other side of the two 50Ohm resistors. Term voltage is -2V for ECL, +3V for PECL.

As termination has to be at the end of line, an analyzer has to have this built in. So for different technology, the user should have programmable control over this to match with technology.

Beside termination the analyzer shall be able to look to the differential input signal on three different ways: differentially, this is most easiest, no need to set a threshold, but not foolproof. In case one DUT output sticks, the other might deliver sufficient signal to switch the analyzer input. This failure can be detected only by checking the differential signal single ended against a threshold (Vcc), once the normal and once the complement signal

R&D measurements

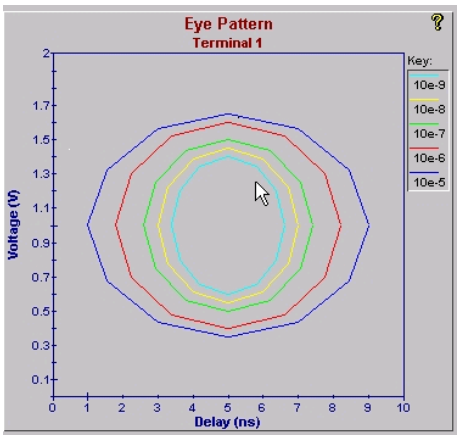
Example: Eye Opening

Characterization:

- **Eye opening (Voltage and Timing)**
- **Optimum sample point**
- **Transition Times**

Results:

- **Graphical Iso BER**
- **Cursors for waveform analysis**



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R&D has to make sure the design works under certain variation of conditions.

This is called characterization, which will answer the question:

'How well does the device work?'

In case of the Eye Opening the parameters of interest are:

•ISO BER, this describes the opening for various BER rates

•optimum sampling point

•Transition times

•Jitter

The picture given is a diagram connecting the points where same BER figures found with a line, different colors show different BER figures.

To make this diagram a lot of measurements have to be completed.

A benefit for the user would be these measurements are automated and the graph shown is drawn out of it by just a mouse click to an Icon within the control software of the test system.

Predefined measurement function for different measurement tasks, called on a mouse click out of the User Interface, make Characterization easier and eliminate various sources for errors.

Manufacturing Measurements

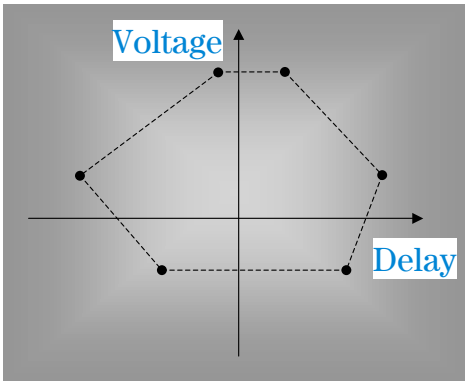
Example: Eye Opening

Verification:

- **6 Point - Eye Contour Measurement**
- **predefined values**
- **fast**

Results:

- **BER at predefined sample points**
- **Pass / fail results**



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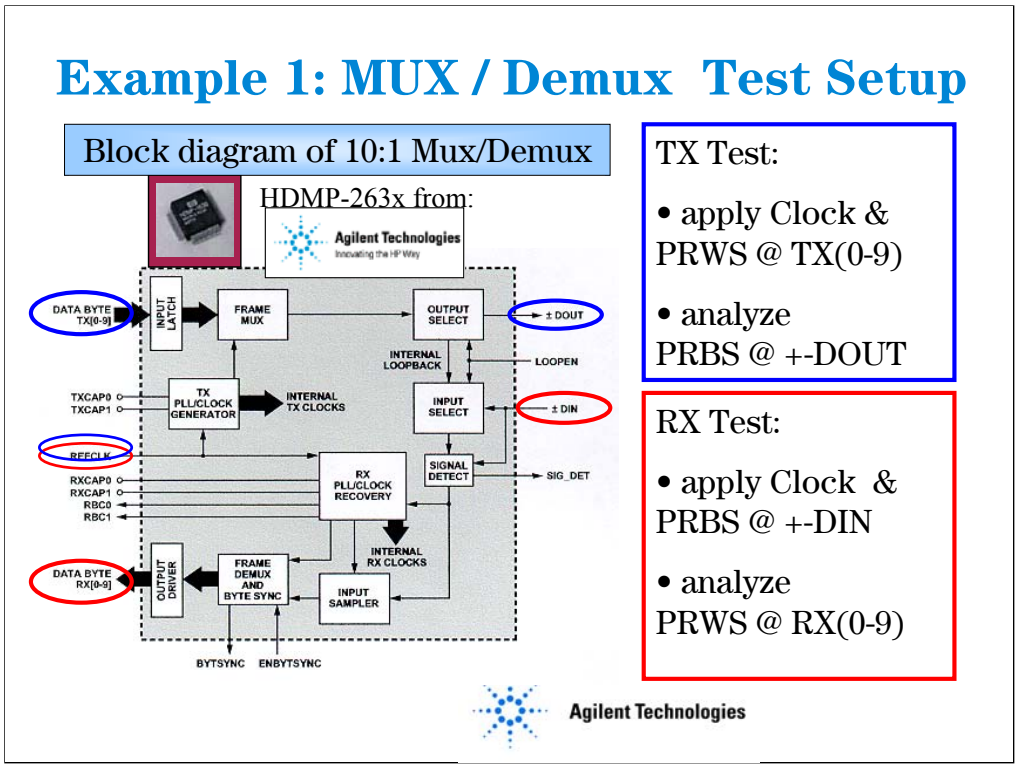
Manufacturing has completely different drivers, here the question is:

• does the DUT meet the specification

• how long does that take

The fastest way of checking the eye opening will be to check the BER at 6 points within the eye. The points will be defined together with the limits for the BER and the measurements function will return a Pass/Fail result.

This measurement function will be fired by remote control. The returned Pass/Fail information will tell the robotics to sort between good and bad parts.



Now we look to the setup of 3 real devices

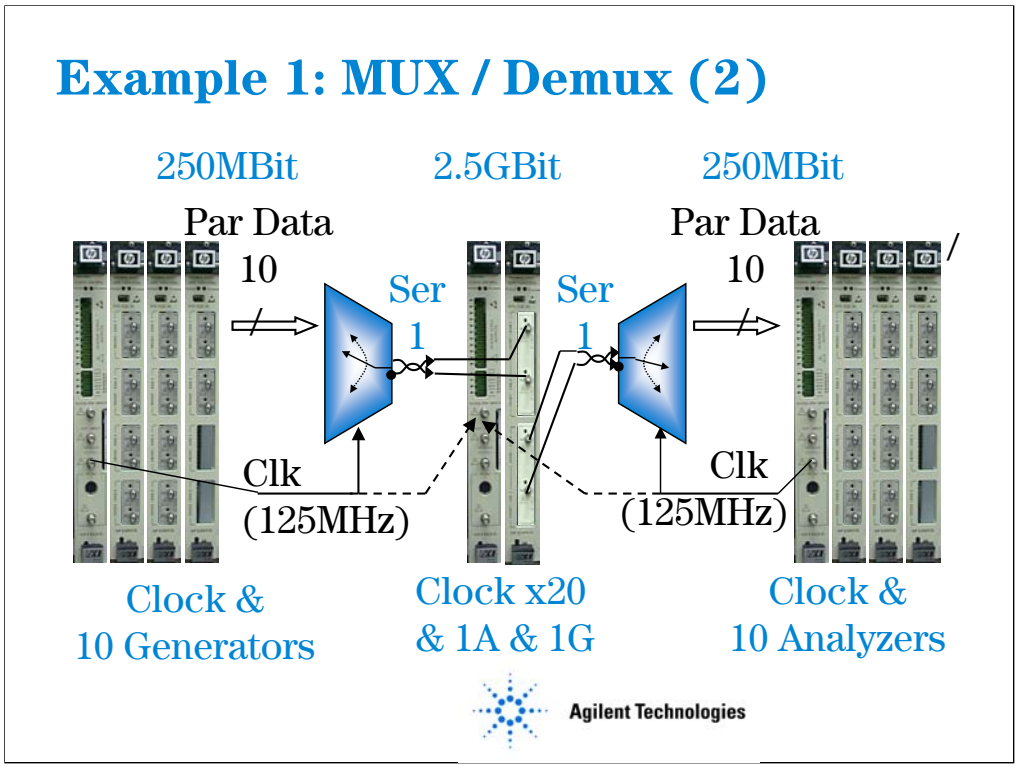
The first example deals with the Gigabit Ethernet Chip from Agilent Technologies. The slide shows the block diagram of this implementation.

TX and RX are both in the same chip. So we look at the two parts consecutively.

TX test needs to apply clock and PRWS data to the inputs. Dout and Ndout (+Dout, -Dout) will be analyzed against PRBS.

RX test need to apply clock and PRBS at Din and nDin (+Din, -Din).

Analyzed will be RX(0-9) against PRWS.



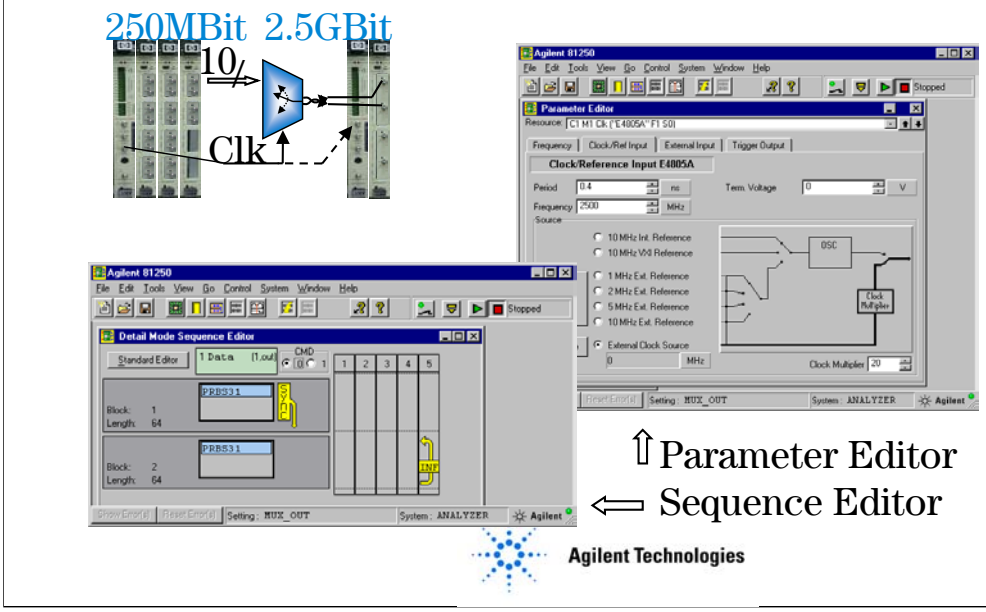
The device needs 250 Mbit/s as parallel data rate and a 125MHz Clock. The serial data rate is 2.5GBit/s.

For analysis or generation of the serial side data, this clock group consisting of a generator and analyzer receives the 125 MHz clock and multiply it internally by a factor of 20. So this is clock synchronous to 2.5 Gbit/s.

The data synchronization will be achieved by the bit synchronization capability of the sequencer.

The parallel side will generate/analyze PRWS data, the serial side will analyze/generate PRBS. Both will use same polynomial.

Example 1: MUX / Demux (3)

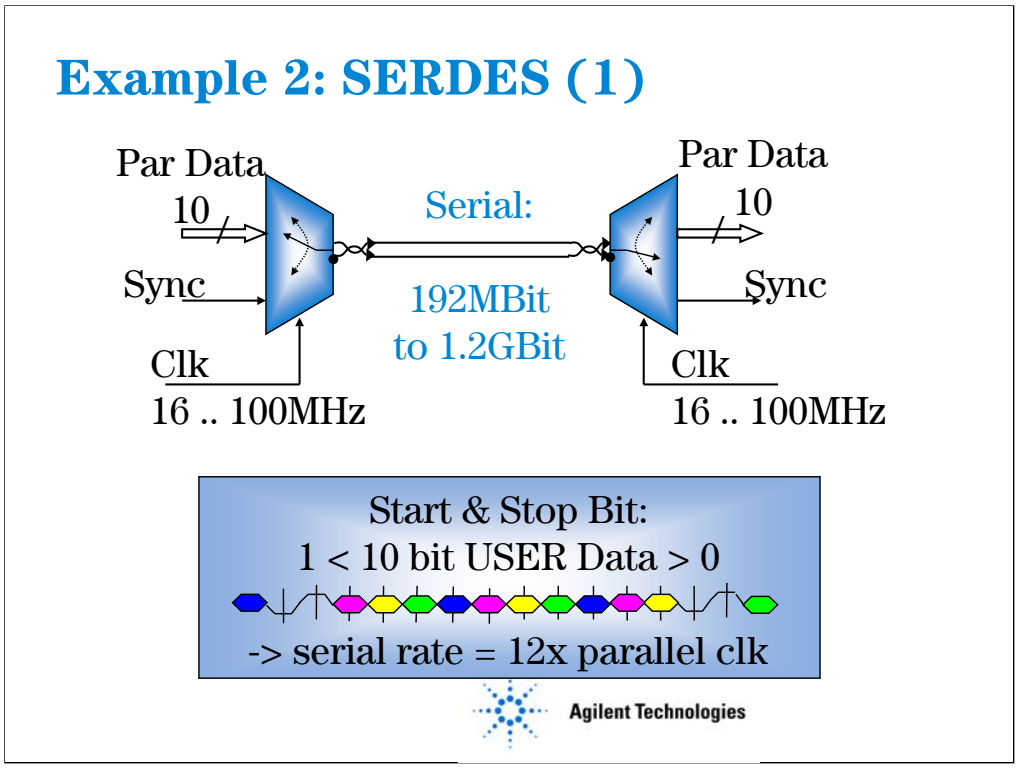


Her we look on two user interface windows showing Parameter editor and Sequence Editor.

The analyzer samples at 2.5GBit/s.

It gets the 125MHz clock and internally multiplies this by 20 shown in the parameter editor.

The data processing is made that first a synchronization takes place to find the proper bit phase and after that he measurement will start.

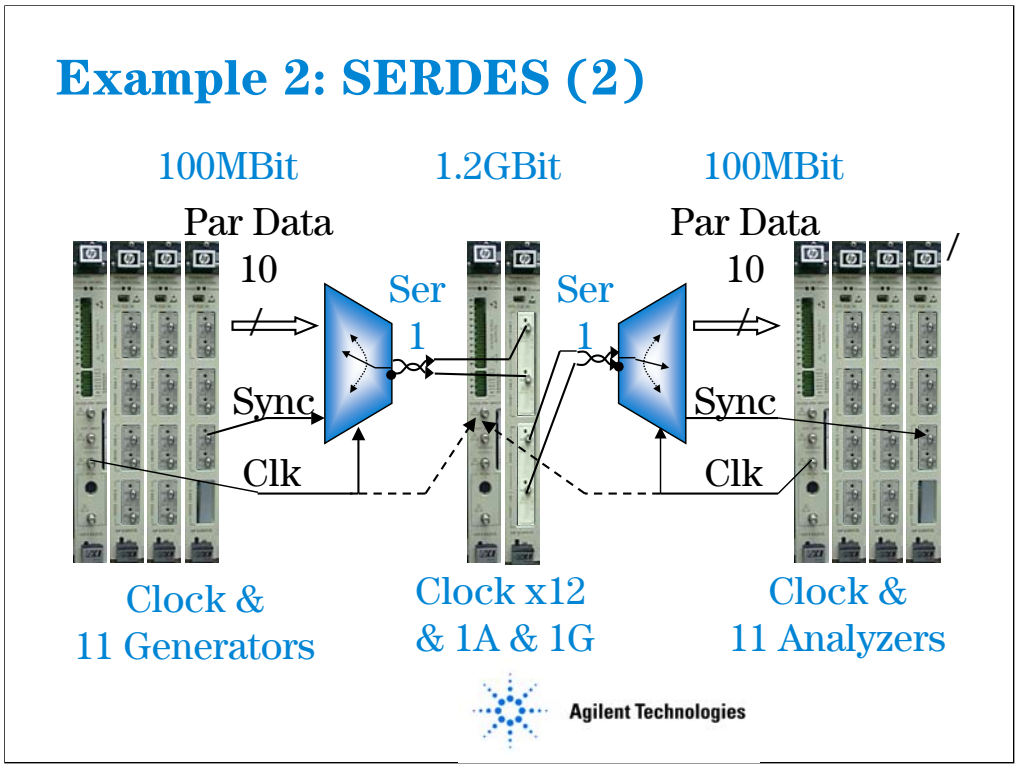


This is the second example: SERDES

This chip works at data rates from roughly 200MBit to 1.2 Gbit on the serial side. The parallel speed is from 10MHz to 100MHz.

Different to the first example is the way how the bits are put together on the serial side: there is a start and stop bit for every 10 user bits. This is also the reason that the serial speed is 12x higher than the parallel side.

With the start stop bit there is a low to high transition guaranteed for every 12 cycles. This is reference for synchronizing the bits on the parallel side of the De-serializer as well there is a minimum of transitions on the link to maintain the clock recovery stable without limitation to the bit combination of the 10 bit blocks of user data.



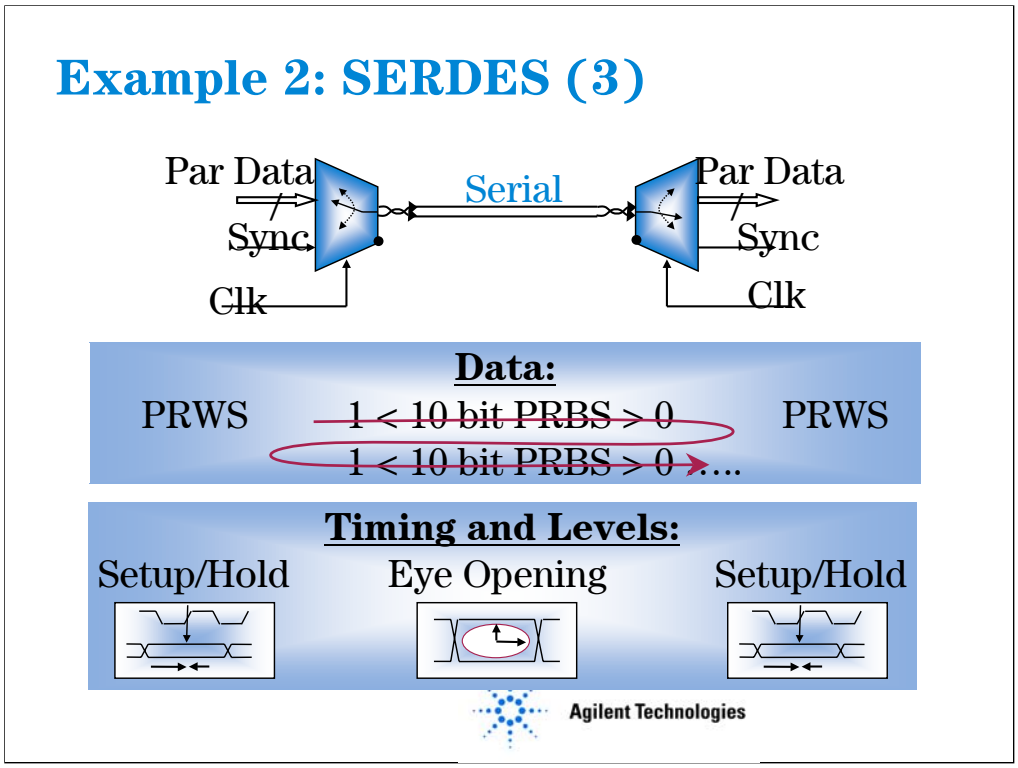
The device needs a 100MHz Clock and 100MBit data flow for 1.2GBit/s data speed on the serial side. Most other is similar to example 1 except the data processing on the serial side:

due to the start stop bits included in the data stream, a pure PRBS based generation/analysis would fail. Instead the bits have to be memory based as the start stop bits cannot be automatically inserted into running PRBS generation.

So it would be most convenient to once capture the data stream from a golden device.

Optional info:

when capturing these kind of data it is important to tailor the captured bit to a segment of proper length. The reason is that PRBS is an odd length by nature (2^n - 1). The memory in the test system is multiplexed: … x16, x 32, x64,… So for proper repeating the segment must have the size of Mux factor times PRBS length + 20% for the start/stop bits.



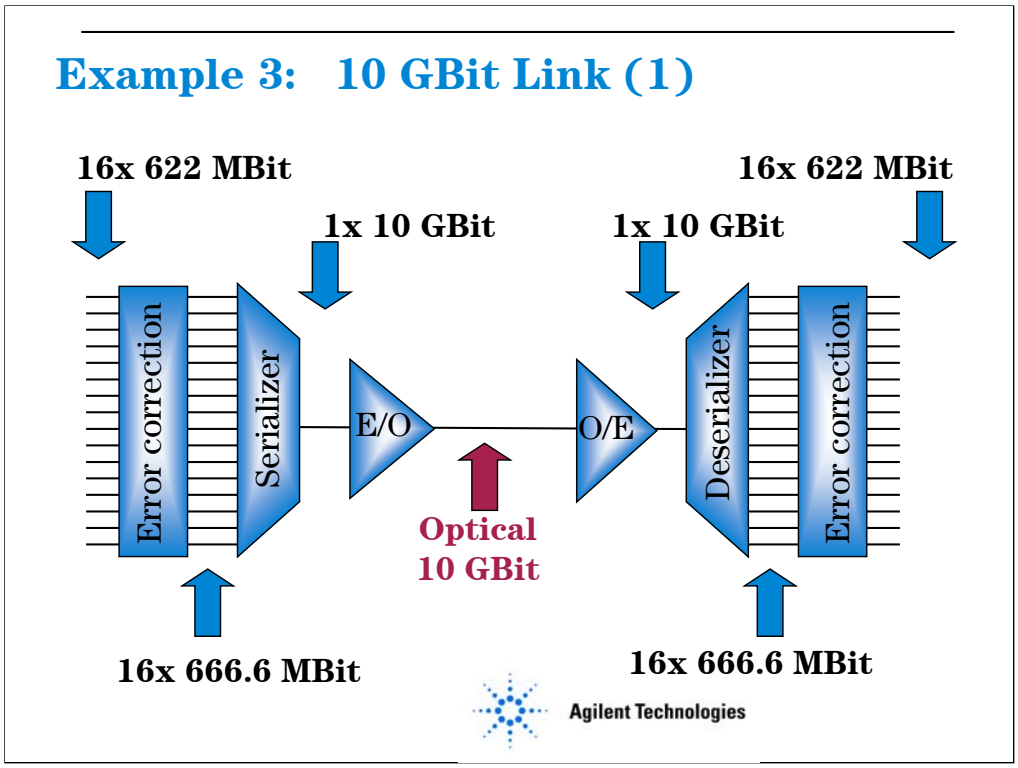
Here we see once again the type of data used on both sides of the SERDES chip. Again the serial side caries a mixture of PRBS and fixed bits. The tester can handles this as data handled memory based. For sure the tester can perform a bit synchronization on this kind of pattern too.

With variable timing and levels per channel, the measurements on the serial and parallel ports can be performed:

•setup and hold times on the parallel side: data valid in reference to the parallel clock

•eye opening on the serial side

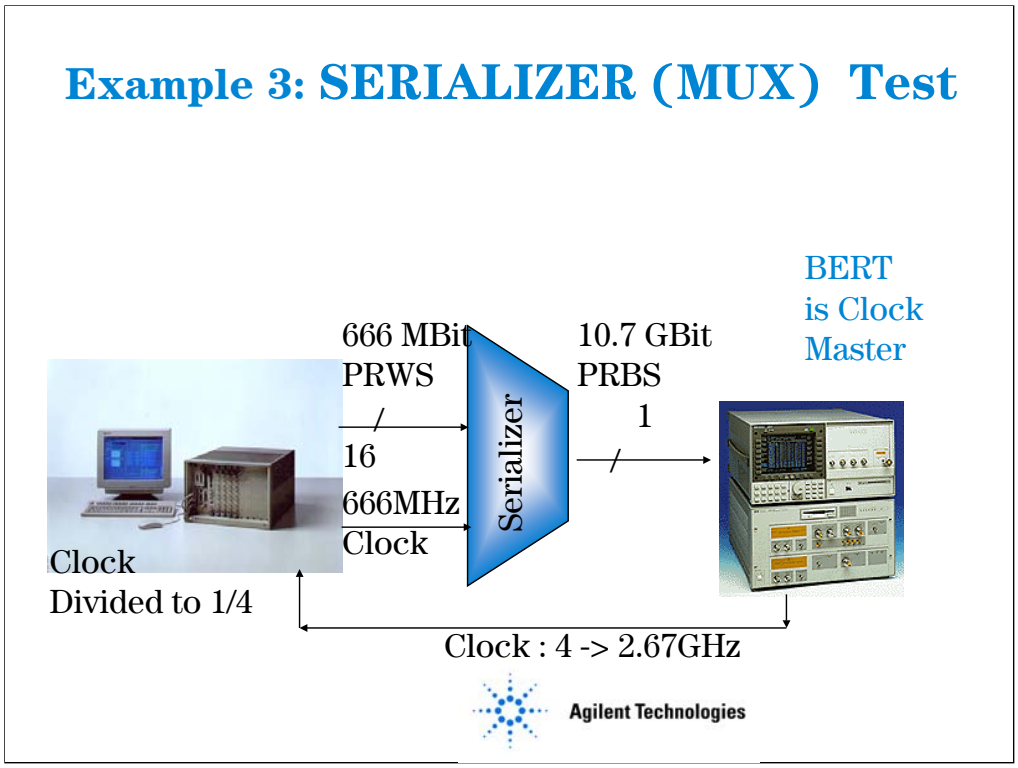
The variable timing and levels would be helpful for R&D characterization as well as manufacturing go/no-go test.



The third example deals with 10GBit on the serial link.

These kind of links working on longer distance use Forward Error Correction (FEC) technology. This technology improves the BER of the total link. It works the way that a certain block of customer data is added by a block of redundant data out of which in case of errors injected at the point of the receiver the errors can be identified and repaired.

So the actual data rate on the serial link is higher due to the overhead. The overhead already adds to the basic data rate of 622MBit to 666 Mbit/s.

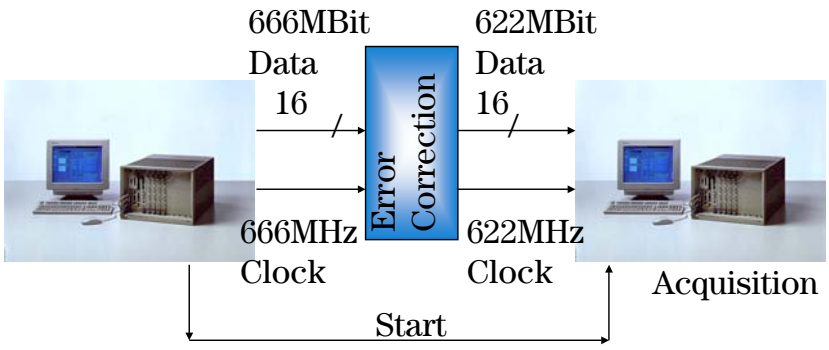


So we look at the different building blocks to be tested isolated:

Here the MUX part is tested with combination of traditional BER test system capable of handling the10.7 GBIt/s. The BERT is clock master, it delivers a clock/4 to the Parbert clock input, which again is internally divided by 4 to generate the PRWS at 666MBit/s.

The De-serializer setup would be same.

Example 3: Error Correction Test



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This is to test the FEC, in this slide this is done for the part on the receiver side. The stimulating pattern includes user and FEC data as a mix. Consequently this is now memory based pattern, which can include multiple errors to check the FEC operation too. On the analyzer side the data can be analyzed by performing a bit synchronization to a known part of the pattern or it can be started by an auxiliary signal (Start) from the generator side or the data can be just acquired for later file processing.

This will work also opposite where the generator stimulates at lower speed providing the user based input data. The analyzer will get the mix of user data and FEC correction data. This can be at least acquired for post processing on file basis.

Summary

81250 ParBERT:
"The Only Parallel Bit-Error-Rate Solution up to 0.66/1.3/2.6 GBit"

- Parallel & Modular
- PRBS, PRWS
- Synchronization
- Individual Timing / Levels per Channel
- differential inputs and outputs (LVDS)

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This are the important issues to make MUX Demux testing successful:

1. Parallel BER test
2. PRBS/PRWS together with bit synchronization
3. Individual timing and levels to make timing changes for and back possible to check for setup / hold times and propagation delay
4. Differential inputs and outputs for e.g. LVDS technology
5. Measurements optimized for use in R&D and manufacturing

Agilent High Speed BERT portfolio

86130A BitAlyzer

ParBERT 81250

SpectralBER

	Serial	Parallel	Parallel Optical
Channels:	1	1-64 Channels	4-64+ Channels optical
Bit Rates:	50M - 3.0/ 3.6 Gbit/s	1M to 2.66 Gbit/s	155M/622M/ 1.25G/ 2.488Gb/s fixed
Size:	Benchtop, like 86100A	VXI	VXI
Target Application:	Telecoms, components etc. Sat Comms, Semicond.	Thorough test of muxes, demuxes and parallel FEC.	Optical Transceiver Test in Manufacturing
Key Features:	86100A compatibility Usability Flexibility	Cost, flexibility, expandability, parallel channels	Low cost/ test optical PRBS & SONET framing

http://www.agilent.com/find/BERT

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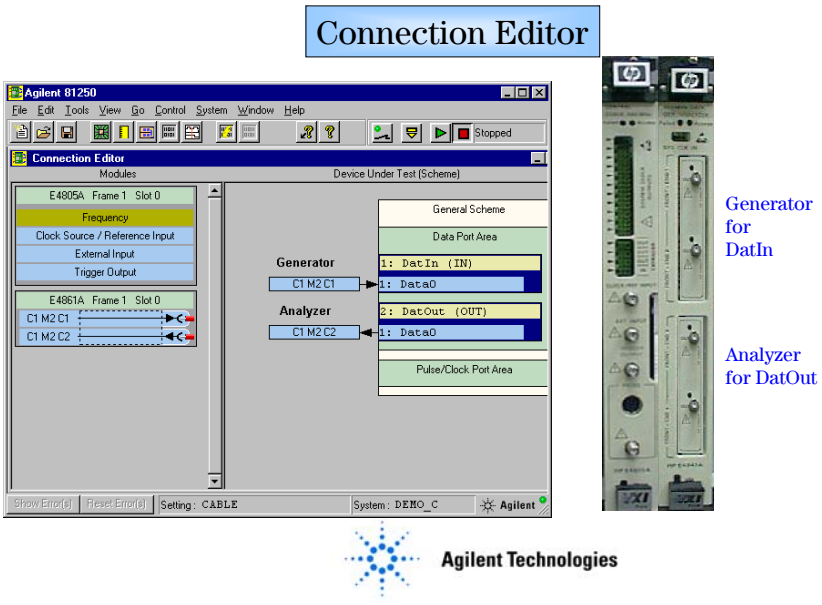
A joined Agilent solution between the ParBERT 81250 and the Spectral BER product offers a scaleable VXI platform ideal for the manufacturing environment. The solution is cost-effective, that allows parallel electrical and optical stimulus and error detection to increase the throughput in your manufacturing environment for multiple and concurrent transmitter and receiver test.

Agilent 81250 Software Screens (1)

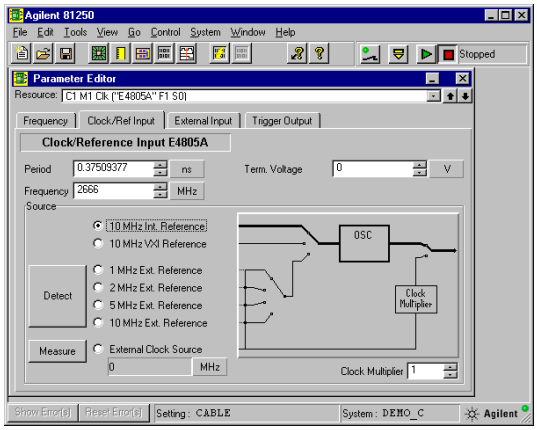


Connection Editor defines virtual DUT and one assigns system resource.

Here is model of a one Generator and Analyzer system how to setup.

Agilent 81250 Software Screens (2)

Frequency and Clock Source



Generator for DatIn

Analyzer for DatOut

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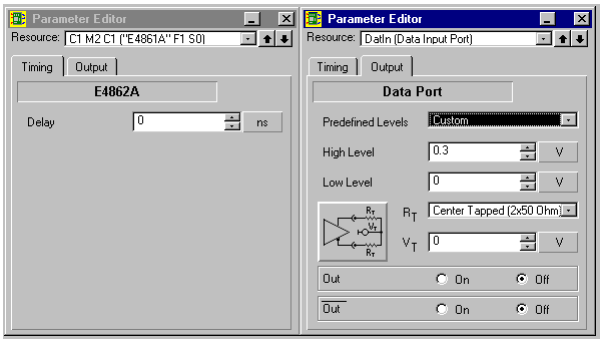
Here one specifies Frequency and Clock Source

Agilent 81250 Software Screens (3)

Generator Timing and Levels



Generator for DatIn

Analyzer for DatOut

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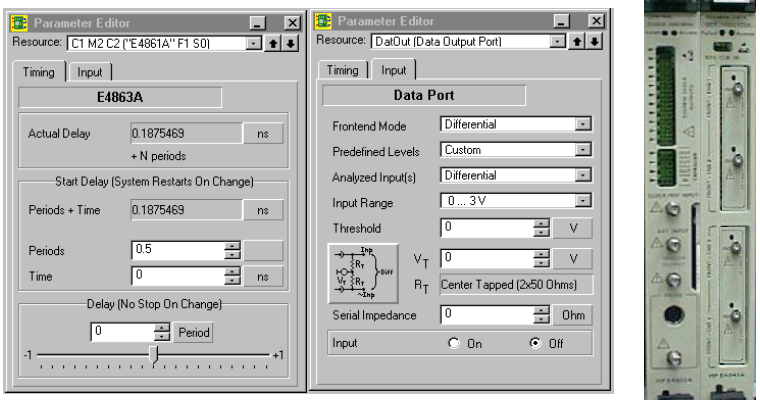
Agilent 81250 Software Screens (4)

Analyzer Sampling and Threshold



Generator for DatIn

Analyzer for DatOut

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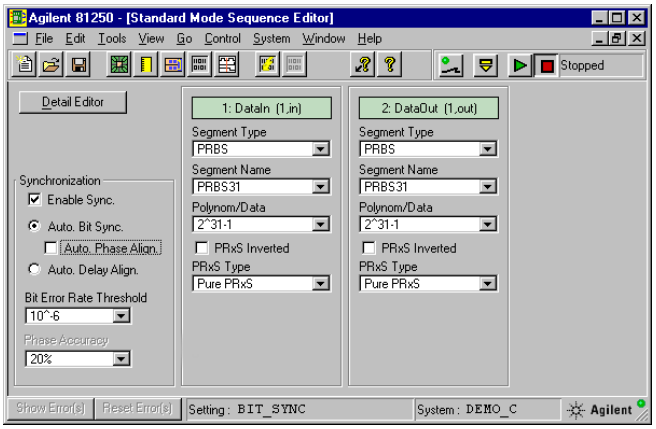
Delay discussion see some slides later

Threshold programming depending on mode, see next slide for termination and measurement mode

Agilent 81250 Software Screens (5)

Standard Sequence Editor



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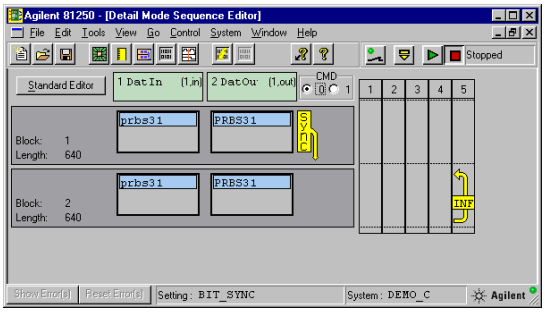
This is ‘Standard’ Editor for Data, Sequencing and Synchronization.

Actually this editor hides sequencing. 81250 shall look like a BERT.

Agilent 81250 Software Screens (6)

Detailed Sequence Editor



Generator for DatIn

Analyzer for DatOut

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This is ‘Detailed’ Editor for Sequencing, known from 81200.

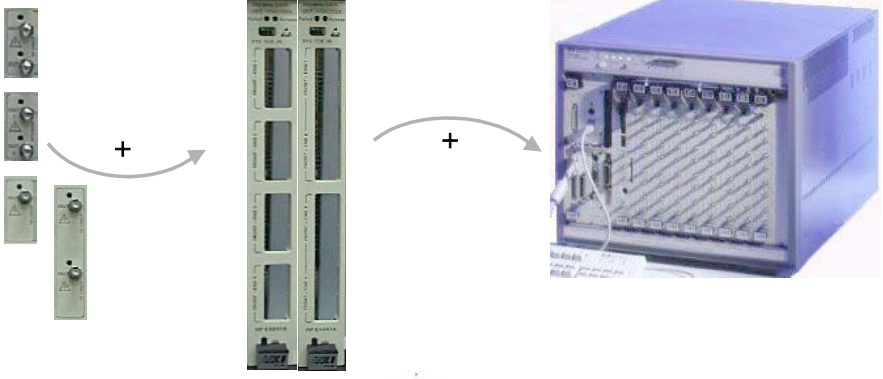
This enables to use all sequencer capabilities like branching on event.

81250 ParBERT Modular HW

Front-Ends :
- type (out/in)
- speed
- # of channels

Modules
- signal processing
- speed &
- # of channels

Mainframe:
- computer interface
- total # of channels



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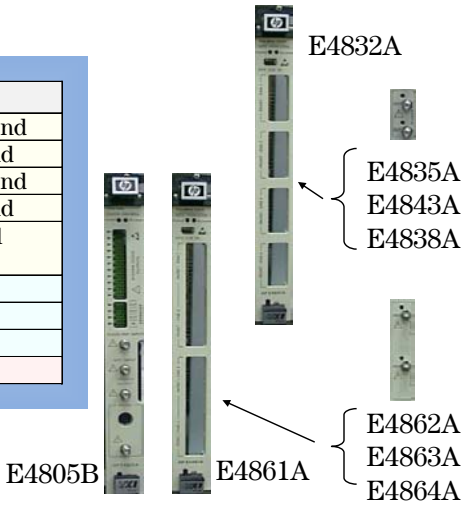
Product Structure

Product	Description
E4862A	2.6 Gbit generator front-end
E4863A	2.6 Gbit analyzer front-end
E4864A	1.3 Gbit generator front-end
E4865A	1.3 Gbit analyzer front-end
E4835A	Dual 660 MHz differential analyzer front-end
E4832A	660 MHz module
E4861A	2.6 Gbit module
E4805B	Central clock module
E4875A	Software revision 3.0



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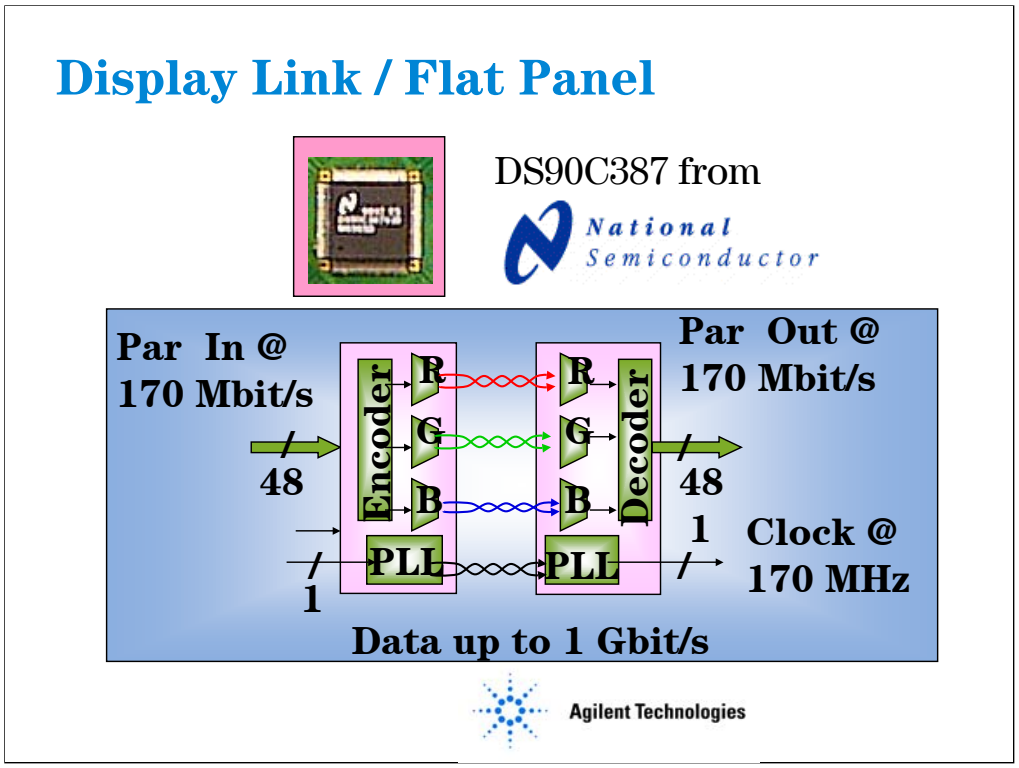


Display Link

There are single silicon CMOS integrated circuits. This note refers to National's DS90C387.

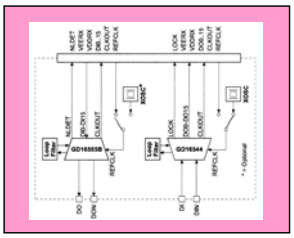
The chips come in a 100-pin PQFP package. Serializer and De-serializer come in independent packages. The total bandwidth is up to 5.38Gbit/s, but this is achieved by up to 8 serial lines. Every Serializer / De-serializer works with 7 parallel lines for in total of 48 RGB data signals.

The serial lines work with LVDS technology.

The points of interest for the designer are:

- Parallel Data to Clock (setup- / hold time)
- Parallel to Serial Data (latency)
- Frequency (32MHz .. 170Mhz)
- Clock Duty Cycle
- Supply Voltage tolerance
- Input sensitivity, Output signal (Eye diagram)
- Jitter (serial out)

10 Gbit/s Transceiver



GD16544/55B from

GIGA

Functional Description :
two bipolar integrated circuits
Multi-layer Ceramic package, 68 pins
SDH STM-64 and SONET OC-192, 10 GBit/s
Serialize / De-serialize in different chips
16 bit wide multiplexing from 622 MHz

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10 Gbit/s Transceiver

This refers to a chipset provided by GIGA. There are two silicon bipolar integrated circuits for TX and RX. They are housed in 68 pin multi-layer ceramic packages. The 10 Gbit/s are used with SONET OC-192 and SDH STM-64. The parallel side is 16 bit wide and operating at 622 MHz.

The points of interest for the designer are the timing parameters:

- Parallel Data to Clock (setup- / hold time)
- Parallel to Serial Data (latency)
- Clock Duty Cycle
- Supply Voltage tolerance
- Input sensitivity, Output signal (Eye diagram)
- Jitter (serial out)

For measurements at the serial side, there is the need for equipment to handle the 10Gbit/s speed.